

REMARKS

Claims 108-121 remain pending.

The Examiner rejected claims 108, 109 and 114-117 under 35 U.S.C. §103(a) as being unpatentable over Satya et al. (US 5,959,459) in view of Chiang et al. (US 6,309,956). Additionally, claims 110, 112, 113, 118, and 120 are rejected under 35 U.S.C. §103(a) as being unpatentable over Satya et al. in view of Chiang et al., and further in view of Huang et al. (US 6,001,733). Claims 111, 119, and 120 are rejected under 35 U.S.C. §103(a) as being unpatentable over Satya et al. and Chiang et al. in view of Huang et al., and further in view of Bennett (US 3,861,023). The Examiner's rejections are respectfully traversed as follows.

Claim 108 is directed towards a "method of fabricating a semiconductor die." Claim 1 also requires "forming a test structure on the semiconductor die, wherein at least a portion of the test structure includes a dummy structure in a top conductive layer, wherein the test structure serves as both a dummy structure and a voltage contrast structure" and "performing voltage contrast testing on the test structure that serves as both a dummy structure and a voltage contrast structure to detect electrical defects within the test structure." That is, testing is performed on a test structure that serves as a VC structure as well as a dummy structure.

The Satya et al. reference is directed towards test structures and methods of performing voltage contrast testing on such VC test structures. The Chiang et al. reference generally teaches how dummy structures can be used along with a low k dielectric to result in a more stable active interconnect structure.

Although Satya teaches voltage contrast (VC) structures and Chiang teaches dummy structures, it is respectfully submitted that these two features cannot be combined since Satya teaches away from using its VC structures as dummy structures. Dummy structures are generally used to fill in the empty spaces of the active device area to provide a more even surface topography so as to minimize chemical mechanical polishing (CMP) problems, such as dishing. For example, Chiang describes typical interconnect structures and their associated problems, such as dishing, with respect to Figs. 1 and 2 and Column 2, Line 59 through Column 3, Line 60. Chiang then goes on to describe a solution for improving the planarity of the structures "[b]y inserting a dummy structure in the open areas." See Column 3, Lines 60-61. Referring to Fig. 2, Chiang specifically states that "the dishing the 232, 240 between groups of metal structures 204, 216, 212 may be avoided by using dummy structures (not shown in Fig. 2)." Chiang then describes useful dummy structures with respect to the remaining Figs. 3A~5. However, these "dummy structures fill up nearby open fields." See Column 4, Lines 8-9. As shown in Figs. 3A

and 3B, the dummy structures can either be placed adjacent to an interconnect structure or surround such structure, respectively. See Column 4, Lines 24-28.

It is also noted that trenches between the dummy structures and active interconnect structures are filled with a low k dielectric material to improve mechanical reliability and improve heat dissipation and that these advantages relate to the low k dielectric material and not the dummy structures themselves. See generally Column 5, Lines 41-56. In other words, the dummy structures only provide improvements to dishing during CMP.

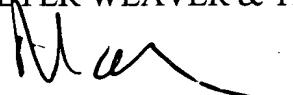
In contrast to dummy structures, the VC structures of Satya are clearly placed in a separate area than the empty spaces of the active region. See Column 1, Lines 29-40 (Emphasis added): “These defect monitors are typically constructed at the same time but *in a different chip location* on the semiconductor substrate than the product VLSI devices, and are discarded once the useful defect information is extracted.” See also Column 3, Lines 43-45: a variety of monitor structures are fabricated *in the dicing-kerf regions* or as a distinct test chip on the semiconductor wafer.” Additionally, the VC structures of Satya are composed of large structure array chains which would not easily fit within a dummy area of the active region. See Fig. 1 and 2.

Since Satya’s VC structure’s are placed in locations that are not suitable for dummy structures (*e.g.*, in the scribe line or on a separate test chip), Satya teaches away from forming dummy structures within its VC structures since dummy structures are necessarily formed in empty regions within the active product region as taught by Chiang and, thus, dummy structures cannot be added to the VC structures of Satya which are not located in such active regions. In other words, the VC structures of Satya cannot fulfill the purpose of dummy structures, which is to reduce dishing during CMP, since the VC structures of Satya are not located in empty spaces of the active region. Accordingly, one would not be motivated to add dummy structures to the VC structures of Satya to alleviate these CMP problems since addition of such dummy structures to the VC structures of Satya would not achieve this goal.

For the forgoing reasons, it is respectfully submitted that claim 108 is patentable over the cited references. The Examiner’s rejections of the dependent claims are also respectfully traversed. However, to expedite prosecution, all of these claims will not be argued separately. Claims 109-121 each depend directly or indirectly from independent claim 108 and, therefore, are respectfully submitted to be patentable over cited art for at least the reasons set forth above with respect to claim 108. Further, the dependent claims require additional elements that when considered in context of the claimed inventions further patentably distinguish the invention from the cited art.

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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